MOTOROLA

MC1391

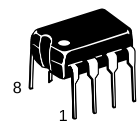
TV Horizontal Processor

The MC1391 provides low–level horizontal sections including phase detector, oscillator and pre–driver. This device was designed for use in all types of television receivers.

- Internal Shunt Regulator
- Preset Hold Control Capability
- ±300 Hz Typical Pull–In
- Linear Balanced Phase Detector
- Variable Output Duty Cycle for Driving Tube or Transistor
- Low Thermal Frequency Drift
- Small Static Phase Error
- Adjustable DC Loop Gain
- Positive Flyback Inputs

TV HORIZONTAL PROCESSOR

SEMICONDUCTOR TECHNICAL DATA

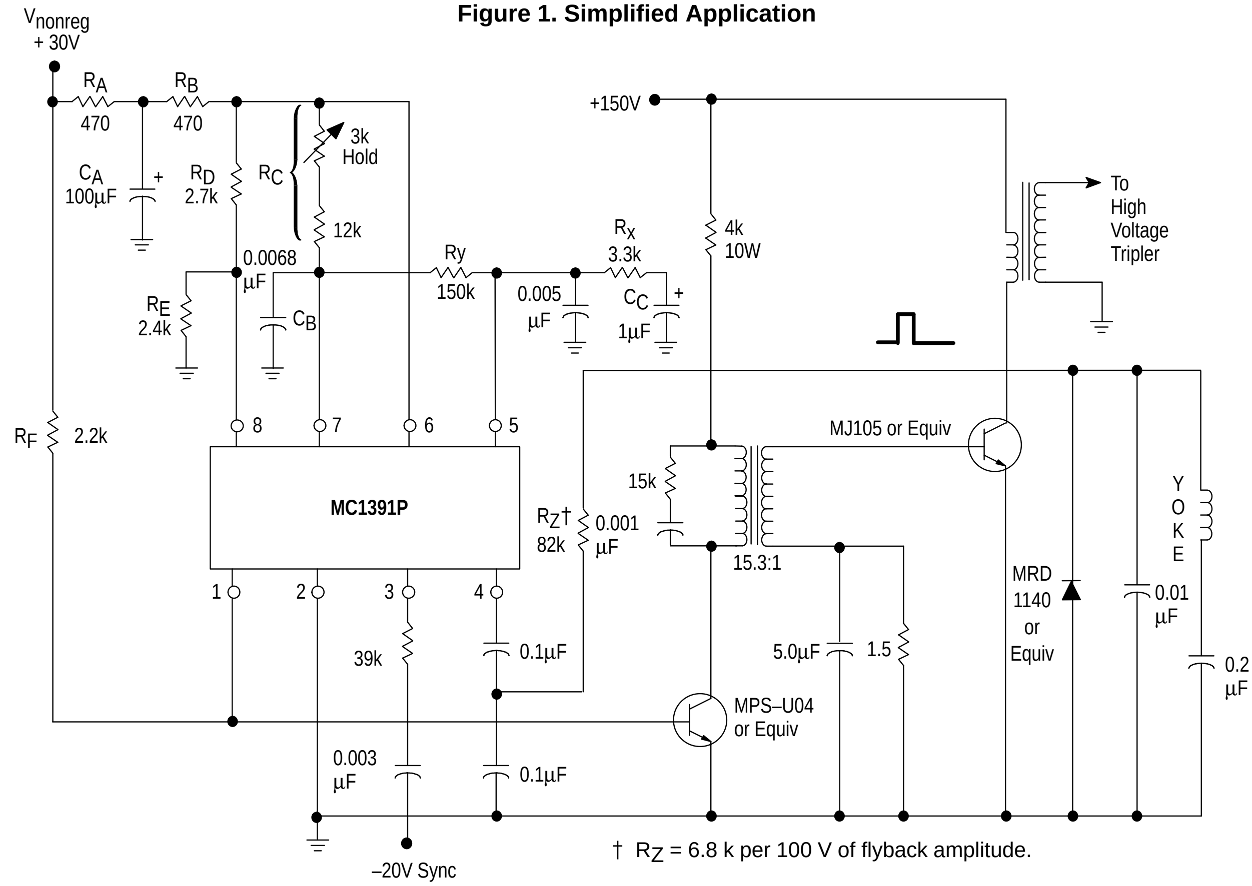


P SUFFIX
PLASTIC PACKAGE
CASE 626

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1391P	T_A = 0° to +70°C	Plastic DIP

Figure 1. Simplified Application



This circuit has an oscillator pull–in range of ±300 Hz, a noise bandwidth of 320 Hz, and a damping factor of 0.8.

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Value	Unit
Supply Current	40	mAdc
Output Voltage	40	Vdc
Output Current	30	mAdc
Sync Input Voltage (Pin 3)	5.0	V_{pp}
Flyback Input Voltage (Pin 4)	5.0	V_{pp}
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +70	°C
Storage Temperature Range	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise noted. See Test Circuit of Figure 2, all switches in position 1.)

Characteristics	Min	Typ	Max	Unit
Regulated Voltage (Pin 6)	8.0	8.6	9.4	Vdc
Supply Current (Pin 6)	–	20	–	mAdc
Collector–Emitter Saturation Voltage (Output Transistor Q1 in Figure 6) (I_C = 20 mA, Pin 1) Vdc	–	0.15	0.25	Vdc
Voltage (Pin 4)	–	2.0	–	Vdc
Oscillator Pull–in Range (Adjust R_H in Figure 2)	–	±300	–	Hz
Oscillator Hold–in Range (Adjust R_H in Figure 2)	–	±900	–	Hz
Static Phase Error (Δf = 300 Hz)	–	0.5	–	µs
Free–running Frequency Supply Dependance (S1 in position 2)	–	±3.0	–	Hz/Vdc
Phase Detector Leakage (Pin 5) (All switches in position 2)	–	–	±1.0	µA
Sync Input Voltage (Pin 3)	2.0	–	5.0	V_{pp}
Sawtooth Input Voltage (Pin 4)	1.0	–	3.0	V_{pp}

Figure 2. Test Circuit

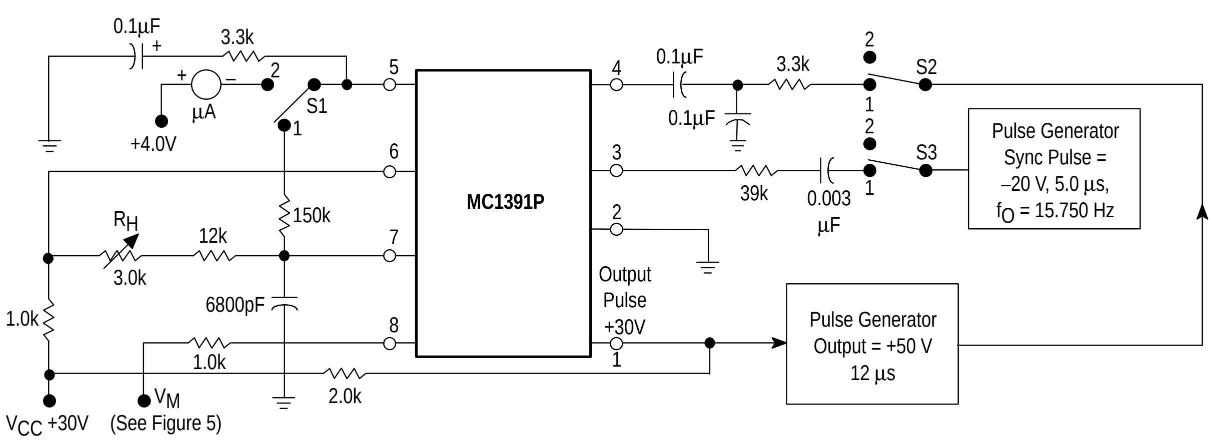


Figure 3. Frequency versus Temperature

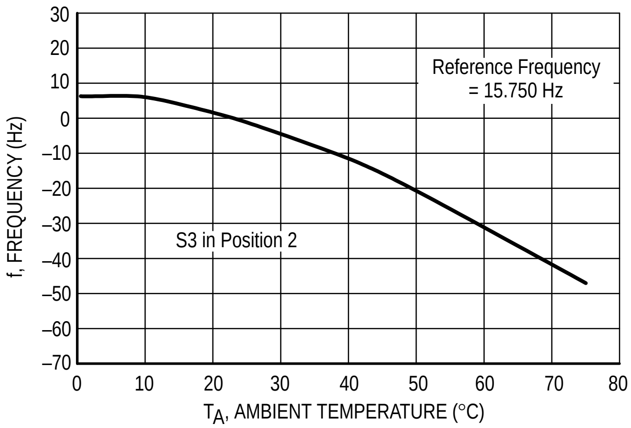


Figure 4. Frequency Drift versus Warm–Up Time

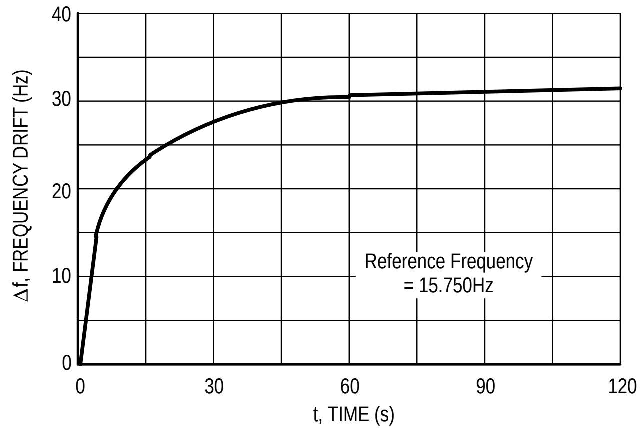


Figure 5. Mark Space Ratio

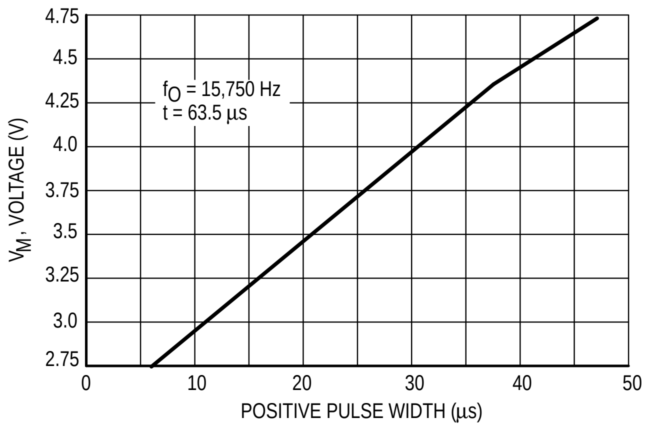
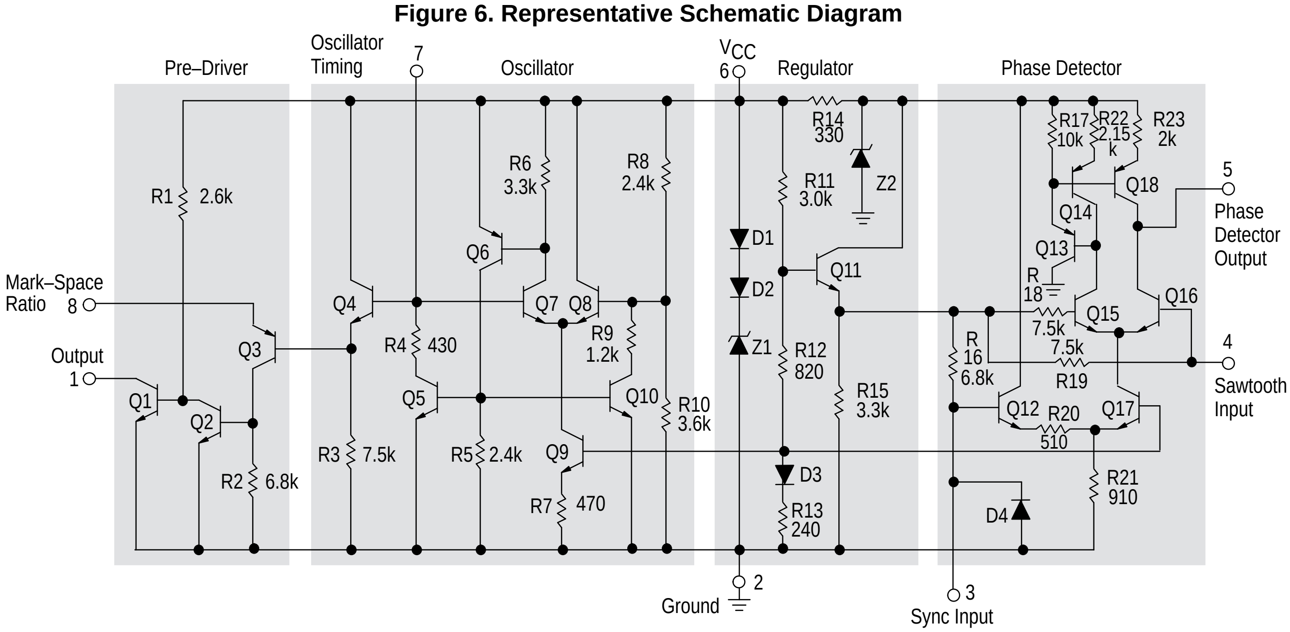


Figure 6. Representative Schematic Diagram



CIRCUIT OPERATION

The MC1391P contains the oscillator, phase detector and predriver sections needed for a television horizontal APC loop.

The oscillator is an RC type with one pin (Pin 7) used to control the timing. The basic operation can be explained easily. If it is assumed that Q7 is initially off, then the capacitor connected from Pin 7 to ground will be charged by an external resistor (R_C) connected to Pin 6. As soon as the voltage at Pin 7 exceeds the potential set at the base of Q8 by resistors R8 and R10, Q7 will turn on and Q6 will supply base current to Q5 and Q10. Transistor Q10 will set a new, lower potential at the base of Q8 determined by R8, R9 and R10. At the same time, transistor Q5 will discharge the capacitor through R4 until the base bias of Q7 falls below that of Q8, at which time Q7 will turn off and the cycle repeats.

The sawtooth generated at the base of Q4 will appear across R3 and turn off Q3 whenever it exceeds the bias set on Pin 8. By adjusting the potential at Pin 8, the duty cycle (MSR) at the predriver output pin (Pin 1) can be changed to accommodate either tube or transistor horizontal output stages.

The phase detector is isolated from the remainder of the circuit by R14 and Z2. The phase detector consists of the comparator Q15, Q16 and the gated current source Q17. Negative going sync pulses at Pin 3 turn off Q12 and the current division between Q15 and Q16 will be determined by the phase relationship of the sync and the sawtooth waveform at Pin 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents will flow in the collectors of Q15 and Q16 each of half the sync pulse period. The current in Q15 is turned around by Q18 so that there is no net output current at Pin 5 for balanced conditions. When a phase offset occurs, current will flow either in or out of Pin 5. This pin is connected via an external low–pass filter to Pin 7, thus controlling the oscillator.

Shunt regulation for the circuit is obtained with a zero temperature coefficient from the series combination of D1, D2 and Z1.

APPLICATION INFORMATION

Although it is an integrated circuit, the MC1391P has all the flexibility of a conventional discrete component horizontal APC loop. The internal temperature compensated voltage regulator allows a wide supply voltage variation to be tolerated, enabling operation from nonregulated power supplies. A minimum value for supply current into Pin 6 to maintain zener regulation is about 18 mA. Allowing 2.0 mA for the external dividers

$$R_A + R_B = \frac{V_{nonreg(min)} - 8.8}{20 \times 10^{-3}}$$

Components R_A, R_B and C_A are used for ripple rejection. If the supply voltage ripple is expected to be less than 100 mV (for a 30 V supply) then R_A and R_B can be combined and C_A omitted.

The output pulse width can be varied from 6.0 µs to 48 µs by changing the voltage at Pin 8 (see Figure 5). However, care should be taken to keep the lead lengths to Pin 8 as short as possible at Pin 1. The parallel impedance of R_D and R_E should be close to 1.0 kΩ to ensure stable pulse widths. For 15 mA drive at saturation

$$R_F = \frac{V_{nonreg} - 0.3}{15 \times 10^{-3}}$$

The oscillator free–running frequency is set by R_C and C_B connected to Pin 7. For values of $R_C \geq R_{discharge}$ (R4 in Figure 6), a useful approximation for the free–running frequency is

$$f_O = \frac{1}{0.6\, R_C C_B}$$

Proper choice of R_C and C_B will give a wide range of oscillator frequencies – operation at 31.5 kHz for countdown circuits is possible for example. As long as the product $R_C C_B \approx 10^{-4}$ many combinations of values of R_C and C_B will satisfy the free–running frequency requirement of 15.734 kHz. However, the sensitivity of the oscillator (β) to control–current from the phase detector is directly dependent on the magnitude of R_C, and this provides a convenient method of adjusting the dc loop gain (fc).

For a given phase detector sensitivity (µ) = 1.60×10^{-4} A/rad

$$fc = \mu\beta \text{ and } \beta = 3.15 \times R_C \text{ Hz/mA}$$

Increasing R_C will raise the dc loop gain and reduce the static phase error (S.P.E.) for a given frequency offset. Secondary effects are to increase the natural resonant frequency of the loop (ω_n) and give a wider pull–in range from an out–of–lock condition. The loop will also tend to be underdamped with fast pull–in times, producing good airplane flutter performance. However, as the loop becomes more underdamped impulse noise can cause shock excitation of the loop. Unlimited increase in the dc loop gain will also raise the noise bandwidth excessively causing horizontal jitter with thermal noise. Once the dc loop gain has been selected for adequate SPE performance, the loop filter can be used to produce the balance between other desirable characteristics. Damping of the loop is achieved most directly by changing the resistor R_X with respect to R_Y which modifies the ac/dc gain ration (m) of the loop. Lowering this ratio will reduce the pull–in range and noise bandwidth (fnn). (Note: very large values of R_Y will limit the control capability of the phase detector with a corresponding reduction in hold–in range.)

Static phasing can be adjusted simply by adding a small resistor between the flyback pulse integrating capacitor and ground. The sync coupling capacitor should not be too small or it can charge during the vertical pulse and this may result in picture bends at the top of the CRT.

Note: In adjusting the loop parameters, the following equations may prove useful:

$$f_{nn} = \frac{1 \times \chi^2 T\omega_C}{4\chi T} \qquad \chi = \frac{RX}{RY}$$

$$w_n = \sqrt{\frac{\omega_C}{(1 + c)T}} \qquad \omega_C = 2\pi fc$$

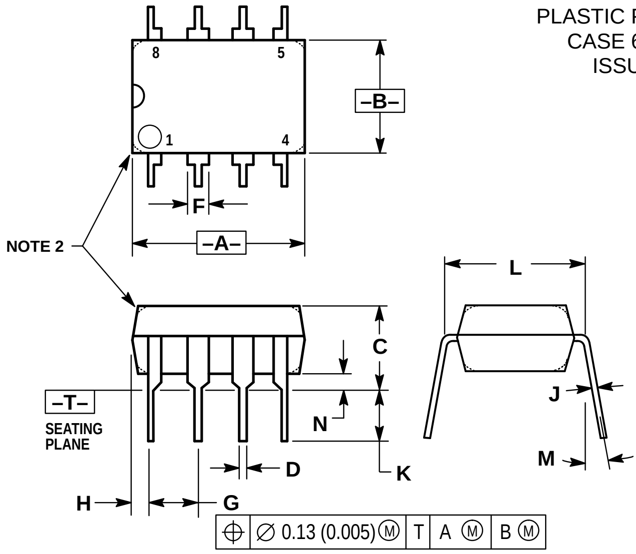
$$T = Ry\,CC$$

$$K = \frac{\chi^2 T\omega_C}{4}$$

where: K = loop damping coeffecient

OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 626–05
ISSUE K



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

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